FAIRCHILD SEMICONDUCTOR™

July 1997
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FST16232
Synchronous 16-Bit to 32-Bit Multiplexer/Demultiplexer Bus Switch

General Description

The Fairchild Switch FST16232 is a 16-bit to 32-bit high-speed CMOS TTL-compatible synchronous multiplexer/demultiplexer bus switch. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

The device allows two separate datapaths to be multiplexed onto, or demultiplexed from, a single path. Two control select pins (S_1, S_0) are synchronous and clocked on the rising edge of CLK when $\overline{\text{CLKEN}}$ is LOW.

Features

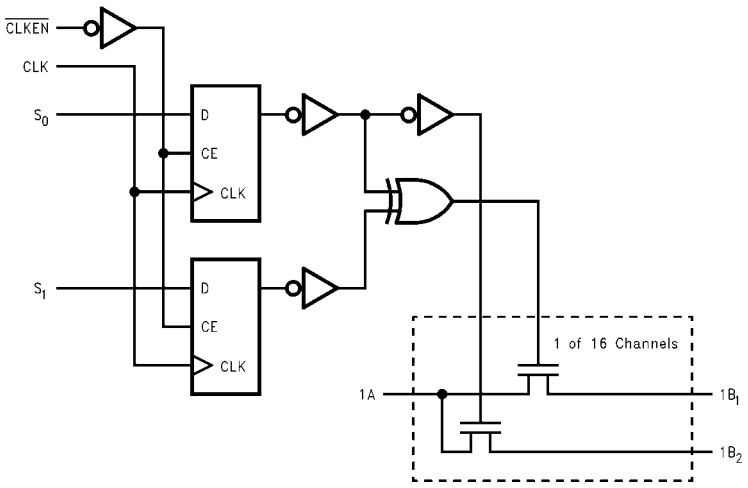
- 4Ω switch connection between two ports.
- Minimal propagation delay through the switch.
- Low I_{CC}.
- Zero bounce in flow-through mode.
- Control inputs compatible with TTL level.

Ordering Code:

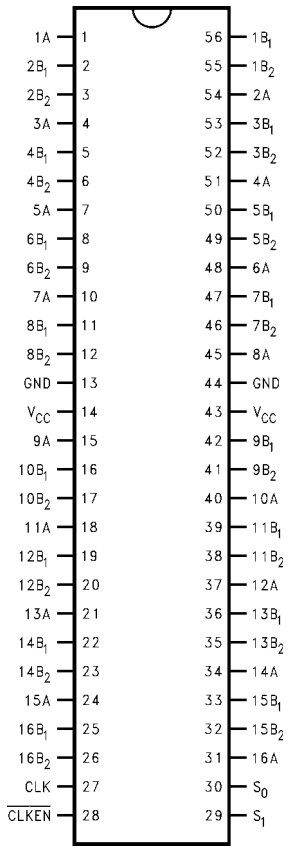
Order Number	Package Number	Package Description
FST16232MEA	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
FST16232MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Diagram



Connection Diagram



Pin Descriptions

Pin Name	Description
S_1, S_0	Control Pins
CLK	Clock Input
$\overline{\text{CLKEN}}$	Clock Enable Input
1A, 2A	Bus A
1B, 2B	Bus B

Truth Table

Inputs				Function
S_1	S_0	CLK	$\overline{\text{CLKEN}}$	
X	X	X	H	Last State
L	L	↑	L	Disconnect
L	H	↑	L	A = B_1 and A = B_2
H	L	↑	L	A = B_1
H	H	↑	L	A = B_2

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Switch Voltage (V_S)	−0.5V to +7.0V
DC Input Voltage (V_{IN})(Note 2)	−0.5V to +7.0V
DC Input Diode Current (I_{IK}) V_{IN}<0V	−50mA
DC Output (I_{OUT}) Sink Current	128mA
DC V_{CC}/GND Current (I_{CC}/I_{GND})	+/− 100mA
Storage Temperature Range (T_{STG})	−65°C to +150 °C

Recommended Operating Conditions (Note 3)

Power Supply Operating (V_{CC})	4.0V to 5.5V
Input Voltage (V_{IN})	0V to 5.5V
Output Voltage (V_{OUT})	0V to 5.5V
Input Rise and Fall Time (t_r, t_f)	
Switch Control Input	0nS/V to 5nS/V
Switch I/O	0nS/V to DC
Free Air Operating Temperature (T_A)	−40 °C to +85 °C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Note 3: Unused control inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = −40 °C to +85 °C			Units	Conditions
			Min	Typ (Note 4)	Max		
V_{IK}	Clamp Diode Voltage	4.5			−1.2	V	I_{IN} = −18mA
V_{IH}	HIGH Level Input Voltage	4.0–5.5	2.0			V	
V_{IL}	LOW Level Input Voltage	4.0–5.5			0.8	V	
I_I	Input Leakage Current	5.5			±1.0	µA	0≤ V_{IN} ≤5.5V
		0			10	µA	V_{IN} = 5.5V
I_{OFF}	OFF-STATE Leakage Current	5.5			±1.0	µA	0 ≤A, B ≤V_{CC}
R_{ON}	Switch On Resistance	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 64mA
	(Note 5)	4.5		4	7	Ω	V_{IN} = 0V, I_{IN} = 30mA
		4.5		8	12	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
		4.0		11	20	Ω	V_{IN} = 2.4V, I_{IN} = 15mA
I_{CC}	Quiescent Supply Current	5.5			3	µA	V_{IN} = V_{CC} or GND, I_{OUT} = 0
ΔI_{CC}	Increase in I_{CC} per Input	5.5			2.5	mA	One input at 3.4V Other inputs at V_{CC} or GND

Note 4: Typical values are at V_{CC} = 5.0V and T_A = +25°C

Note 5: Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40\,°C$ to $+85\,°C$, $C_L = 50pF$, $RU = RD = 500\Omega$				Units	Conditions	Figure No.
		$V_{CC} = 4.5 - 5.5V$		$V_{CC} = 4.0V$				
		Min	Max	Min	Max			
f_{MAX}	Maximum Clock Frequency	150		150		MHz	V_I = OPEN	Figure 1 Figure 2
t_{PHL}, t_{PLH}	Prop Delay Bus to Bus (Note 6)		0.25		0.25	ns	V_I = OPEN	Figure 1 Figure 2
t_{PHL}, t_{PLH}	Prop Delay CLK to B or A	2.0	6.3		6.0	ns	V_I = OPEN	Figure 1 Figure 2
t_{PZH}, t_{PZL}	Output Enable Time CLK to A = B_1 = B_2	1.7	8.5		9.0	ns	V_I = 7V for t_{PZL}, V_I = OPEN for t_{PZH}	Figure 1 Figure 2
	Output Enable Time CLK to A or B_1 or B_2	2.0	6.5		6.5	ns	V_I = 7V for t_{PZL}, V_I = OPEN for t_{PZH}	Figure 1 Figure 2
t_{PHZ}, t_{PLZ}	Output Disable Time CLK to A or B	1.0	8.5		9.0	ns	V_I = 7V for t_{PLZ}, V_I = OPEN for t_{PHZ}	Figure 1 Figure 2
t_S	Setup Time S_1, S_0 before CLK ↑	2.5		2.8		ns		Figure 1 Figure 2
	Setup Time $\overline{CLKEN}$ before CLK ↑	1.8		2.0				
t_H	Hold Time S_1, S_0 after CLK ↑	1.0		1.0		ns		Figure 1 Figure 2
	Hold Time $\overline{CLKEN}$ after CLK ↑	1.5		1.5				
t_W	Pulse Width	3.1		3.1		ns	Clock HIGH or LOW	Figure 1 Figure 2

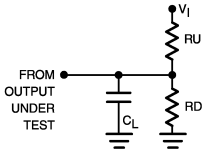
Note 6: This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).

Capacitance (Note 7)

Symbol	Parameter	Typ	Max	Units	Conditions
C_{IN}	Control pin Input Capacitance	4		pF	V_{CC} = 5.0V
$C_{I/O}$	Input/Output Capacitance	7		pF	V_{CC} = 5.0V, S_0, S_1 = 0V

Note 7: $T_A = +25°C$, f = 1 MHz, Capacitance is characterized but not tested.

AC Loading and Waveforms



Note: Input driven by 50 Ω source terminated in 50 Ω

Note: C_L includes load and stray capacitance

Note: Input PRR = 1.0 MHz, t_W = 500 ns

FIGURE 1. AC Test Circuit

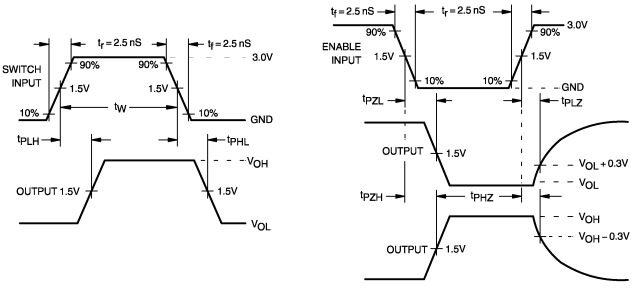
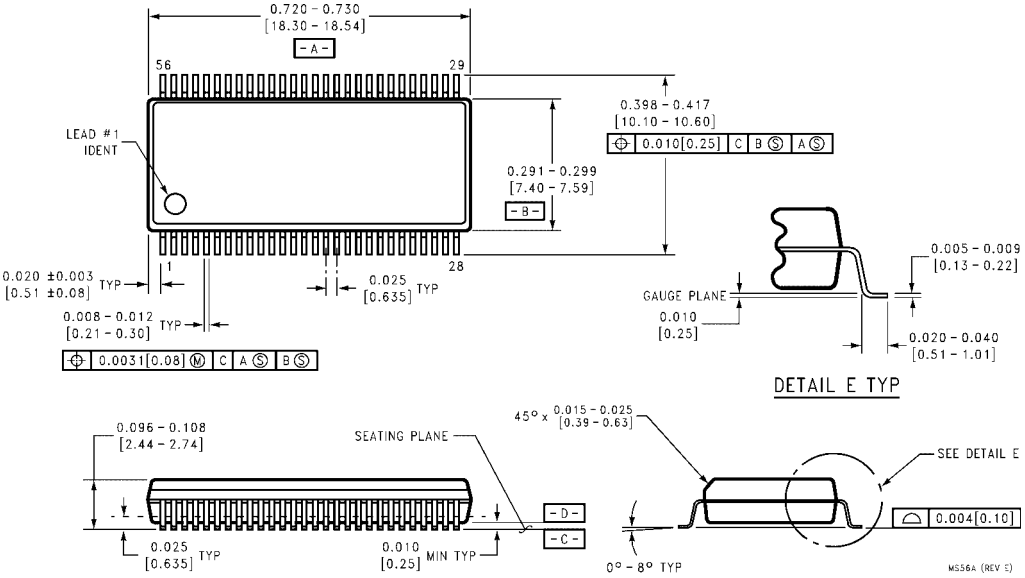


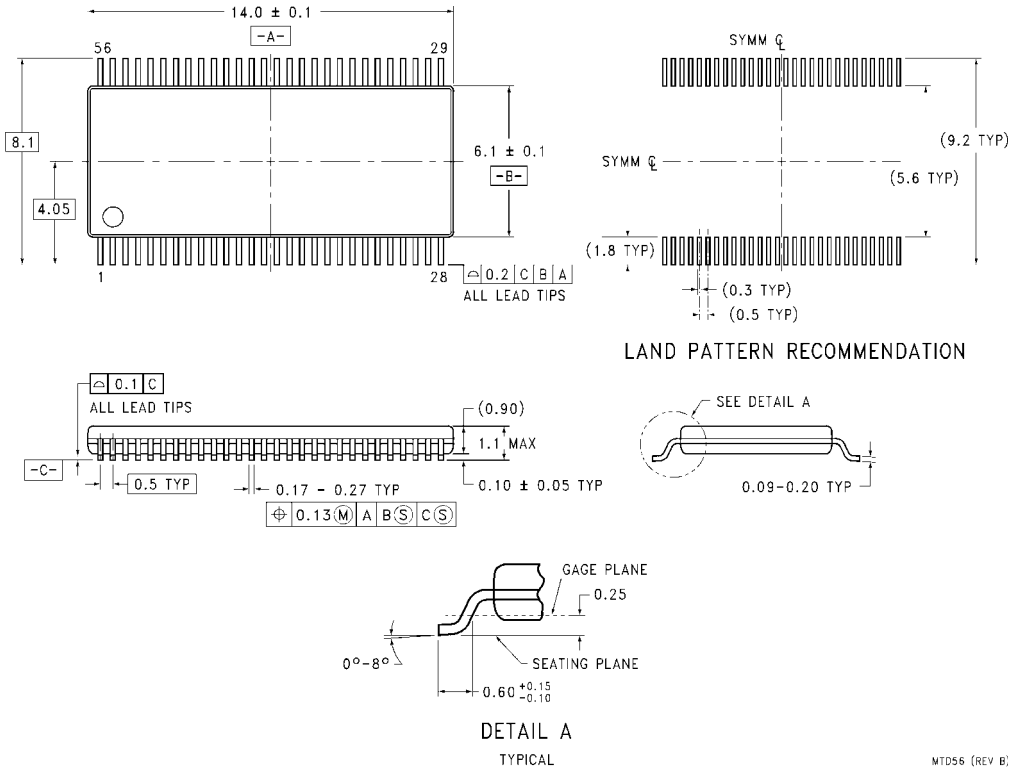
FIGURE 2. AC Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted



56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
Package Number MS56A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

Technology Description

The Fairchild Switch family derives from and embodies Fairchild's proven switch technology used for several years in its 74LVX3L384 (FST3384) bus switch product.